Attorney's Docket No.: 10559-348001/P9836

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : McCall et al. Art Unit: 2181
Serial No.: 09/666,489 Examiner: Glen Allen Auve
Filed : September 18, 2000
Title : BUFFERING DATA TRANSFER BETWEEN A CHIPSET AND MEMORY MODULES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.131

We, James A. McCall, a United States citizen residing in Beaverton, OR, Randy M. Bonella, a United States citizen residing in Portland, OR, John B. Halbert, a United States citizen residing in Beaverton, OR, Jim M. Dodd, a United States citizen residing in Shingle Springs, CA, and Chung Lam, a United States citizen residing in Redwood City, CA, hereby declare as follows:

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

April 30, 2004
Date of Deposit

Carroll L. Allman
Signature

Carroll Allman
Typed or Printed Name of Person Signing Certificate

1. That we are the co-inventors of the subject matter disclosed and claimed in the above-referenced U.S. patent application.

2. That we have read the present claims of this application, which are directed to methods and systems dealing with interfaces between chipsets and memory modules.

3. That we understand that the Lai application claims the priority of United States Provisional Application Serial No. 60/211,095 filed on June 12, 2000 (hereinafter the "Lai provisional application").

4. That prior to June 12, 2000, and thus necessarily before the filing date of the Lai provisional application, we had worked in the United States of America on the subject matter recited in the present claims.

5. We submit herewith, as Exhibit A, eight pages of a presentation created on March 29, 2000 and subsequently presented within one week at a meeting attended by our supervisor, Pat Gelsinger, an employee of Intel Corporation. The creation and presentation thus occurred prior to the June 12, 2000 filing date of the Lai provisional application. The Independent Memory Architecture (IMA) concept first described on page 2 of Exhibit A shows a memory interface and methods involving the memory interface.

6. We submit herewith, as Exhibit B, eight pages of a waveforms describing operations of the IMA. The waveforms were last modified on March 29, 2000, prior to the June 12, 2000 filing date of the Lai provisional application.

7. Exhibit A describes and summarizes the IMA concept including the provision of buffers in an interface between a chipset and memory modules. The buffers allow the interface to be split into sub-interfaces and latch data transferred between the chipset and the memory modules. The sub-interfaces operate independently but in synchronization with each other. The IMA allows the sub-interfaces to operate at different voltage levels and different frequencies.

8. Exhibit B describes and summarizes operational modes of an implementation of the IMA concept.

9. That we hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Date: 4/16/03

James A. McCall

Date: 4/19/2004

Randy M. Bonella

Date: 3/30/2004

John B. Halbert

Date: _____

Jim M. Dodd

Date: _____

Chung Lam

10367236.doc

Respectfully submitted,

Date: _____

James A. McCall

Date: _____

Randy M. Bonella

Date: _____

John B. Halbert

Date: 4/19/04

Jim M. Dodd

Date: _____

Chung Lam

10367236.doc

Respectfully submitted,

Date: _____

James A. McCall

Date: _____

Randy M. Bonella

Date: _____

John B. Halbert

Date: _____

Jim M. Dodd

Date: 4/19/2004

Chung Lam

10367236.doc

Exhibit A

ADT Technical Update

Key Accomplishments

- Technical/Performance Targets Bought-Off By ADT Members
  - 6.4GB/sec Per Channel (4X RDRAM Single Channel)
  - 2GB Maximum Memory Per Channel
  - 2 Double-Sided Modules
  - Targeting High-End/Mainstream DT
- Technical Timeline Bought-Off By ADT Members
  - Initial Samples Q3'02
  - Launch Q1'04
  - Timeline Based On Known Risks and Past History

ADT Technical Issues

Platform Memory Organization

There Are Several Key Areas Where Intel and DRAM Suppliers Have Conflicting Requirements.

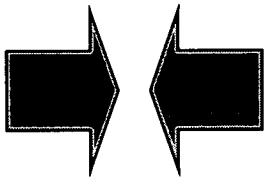
Intel

Need ≤ 1V Maximum Voltage Signaling

- May Need Diff. Signaling

Need Narrow Interface To Allow Integration Into CPU And To Reduce C/S Cost

- Implies High Frequency To Achieve 6.4GB/sec



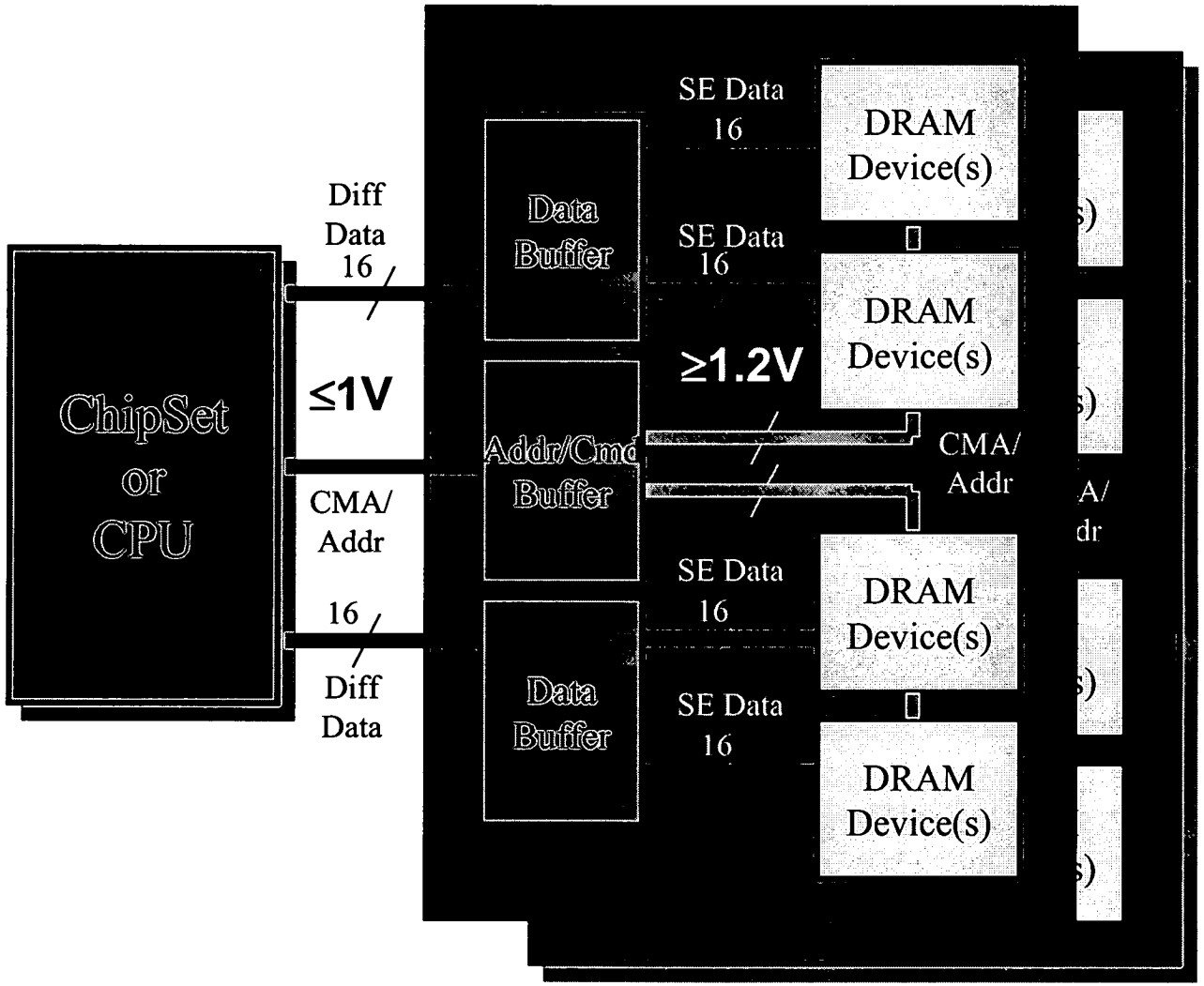
Suppliers

- Need ≥1.2V Maximum Voltage Signaling
  - Prefer 1.5-1.8V
- Need Lower Frequency To Reduce Tester Cost
  - ≤ 800Mb/pin/sec
  - Implies Wide Interface
- Need Single-Ended Signaling For Low Pin-Count

IMA Concept

Platform Memory Organization

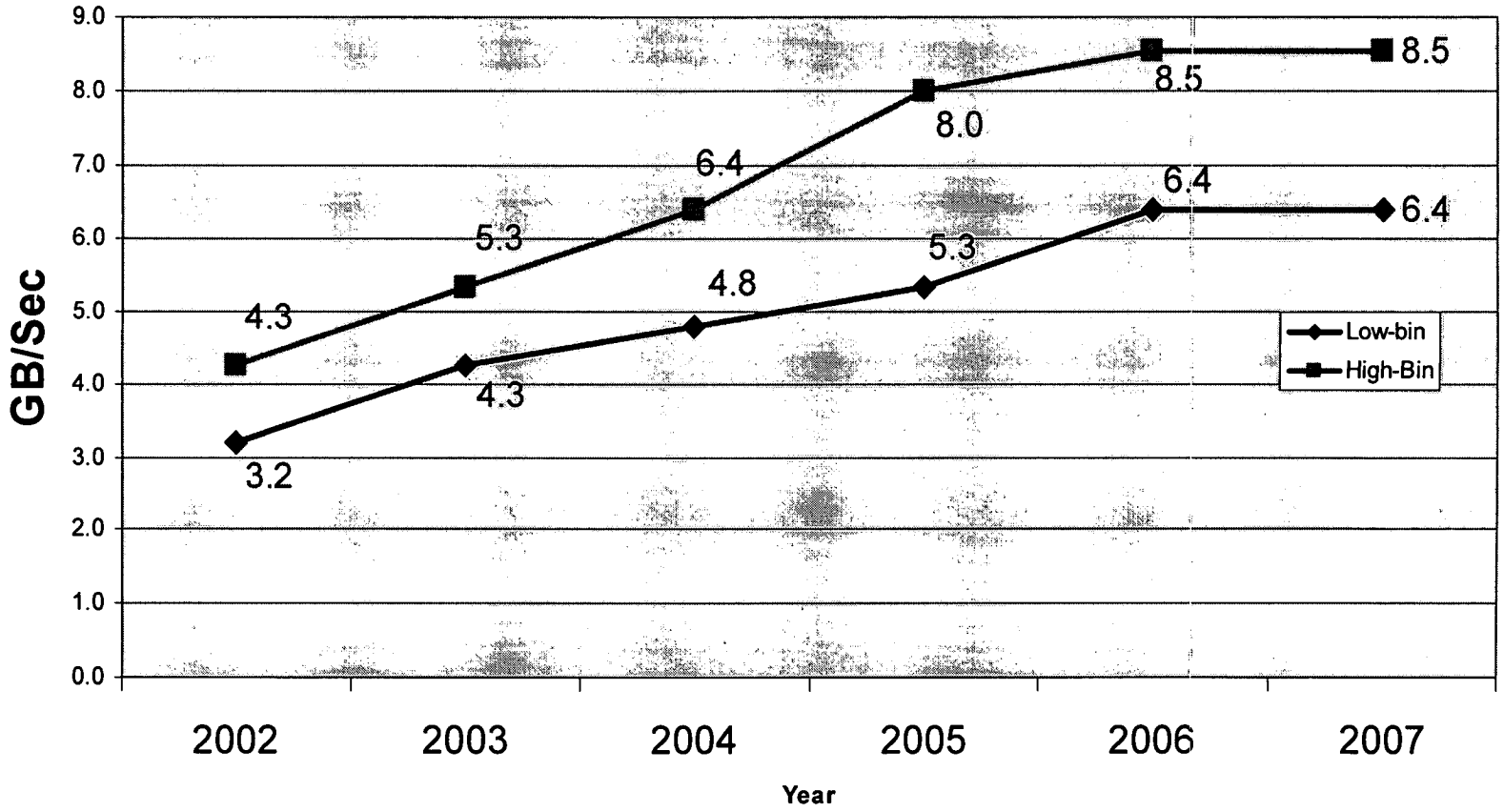
IMA = Independent Memory Architecture



- **IMA Buffers Allow For Each Side To Optimize Voltage, Signaling and Frequency Independently**
- **Enables Performance Targets**
- **Eliminates Conflicting Requirements**

IMA Buffers Isolate Controller From DRAM Devices

IMA BW Roadmap

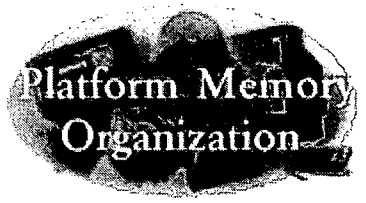


IMA Latency Estimates

	CPU Rd Latency (CPU Bus Clocks)		
Technology	Page-Hit	Page-Empty	Page-Miss
PC133	8	10	12
PC800 D-RDRAM	10	12	14
ADT-4200	9	11	13
ADT-6400	8	10	12
ADT-8400	8	10	12

- Based on 133MHz CPU FSB Clock (Northwood Derivative)
- Estimated ADT Latency Less Than PC800 D-RDRAM
  - Assumes Full-Clock Retiming Through Buffers
    Latency Can Be Further Improved In Some Cases

IMA Compatibility



The Best Chance For Backward Compatibility Is With DDR

Two possible ways of positioning compatibility

Compatibility Scenario #1:

- Same Platform Can Boot With Either ADT Or DDR
- Mostly Pin Compatible (assuming 32-bit differential)
  - ADT Probably Has More Control Pins
- Electricals Of ADT May Preclude Interoperability On One MB

Compatibility Scenario #2:

- Different Platform, Same C/S
- Pin Compatible, Electricals Probably Workable

Segmentation

Segment

Mid-Range/HE Server

- Dual Channel,4.2-6.4 GB/Sec Per Channel (8.4-12.8 GB/sec total)
- 2 Modules Per Channel (8GB Total w/ x4 512Mb)
- ***Need To Address Density Strategy***

Entry Server

- Dual Channel,3.2-4.2 GB/Sec Per Channel (6.4-8.4 GB/sec total)
- 2 Modules Per Channel (8GB Total w/ x4 512Mb)

H/E, Mainstream DT

- Single-Channel, 4.2-6.4GB/Sec
- 2 Modules Max (2GB w/512Mb)

Value DT

- Single-Channel, 3.2 GB/Sec
- 1-2 Modules

Mobile

- Single Channel, 3.2-4.2GB/Sec
- 2 Modules (1GB w/ x16 512Mb)
- Target is 2.5W For Memory Sub-system

C/S Schedule Scenarios

Platform Memory Organization

- Scenario #1: Design From Scratch (Based on 820 B/C Schedule)
  - PIP To A-0 T/: 4 Quarters
  - A-0 To Prod. T/O: 2 Quarters

  Start PIP in Q3'00

  Production: Q1'02

  Implies BTS'02

Scenario #2: "Quick and Dirty" Based on i810e and 440GX Schedules

- PIP To A-0 T/: 2 Quarters
- A-0 To Prod. T/O: 2 Quarters

Start PIP in Q3'00

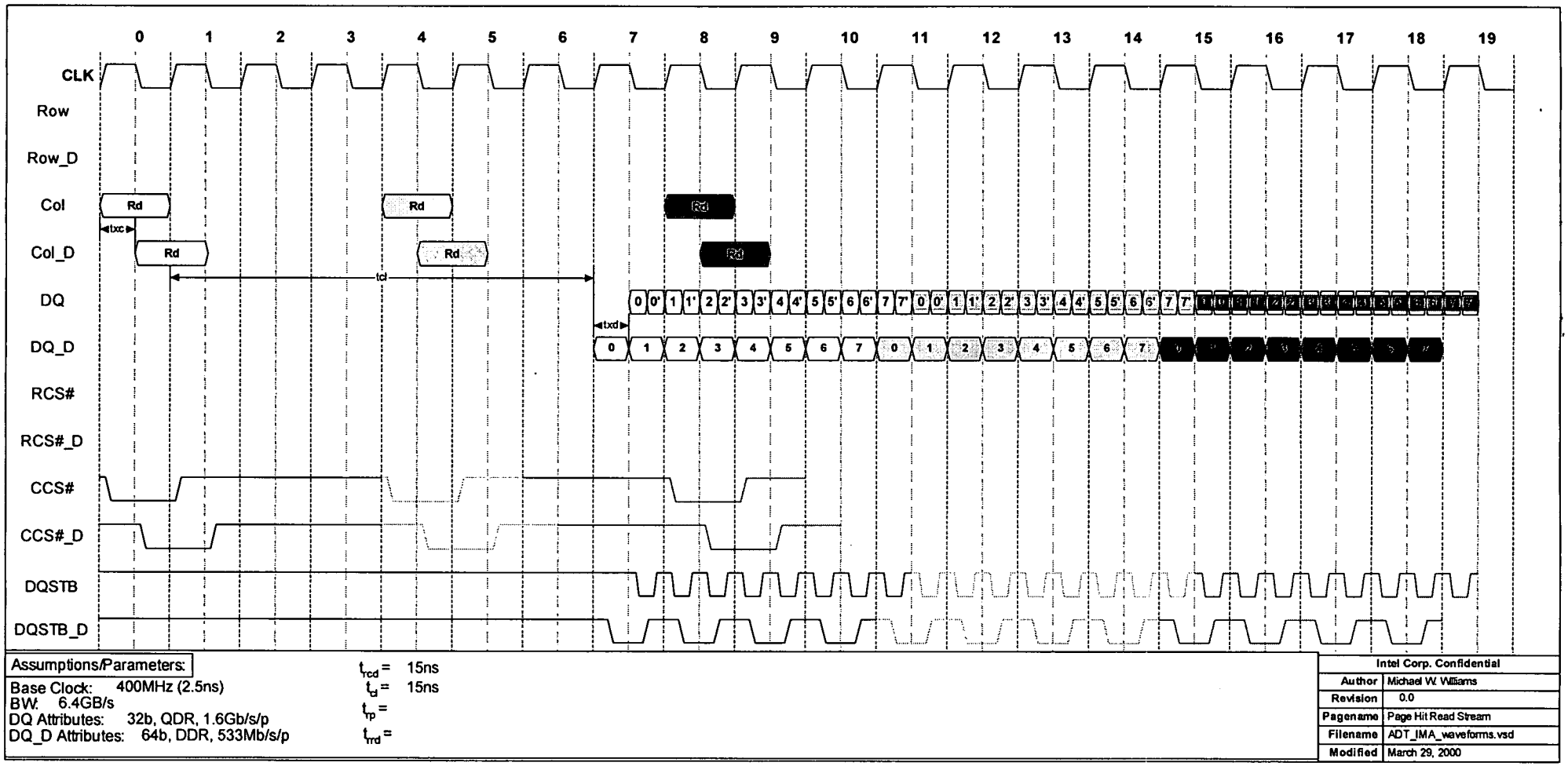
Production: Q3'01

Implies Spring Refresh '02 (Maybe Holiday Refresh '01)

Indicates a '01 Production Is Unlikely (Probably Impossible)

Assumes Q3'00 Start To Work Which Is Probably Agressive

Exhibit B



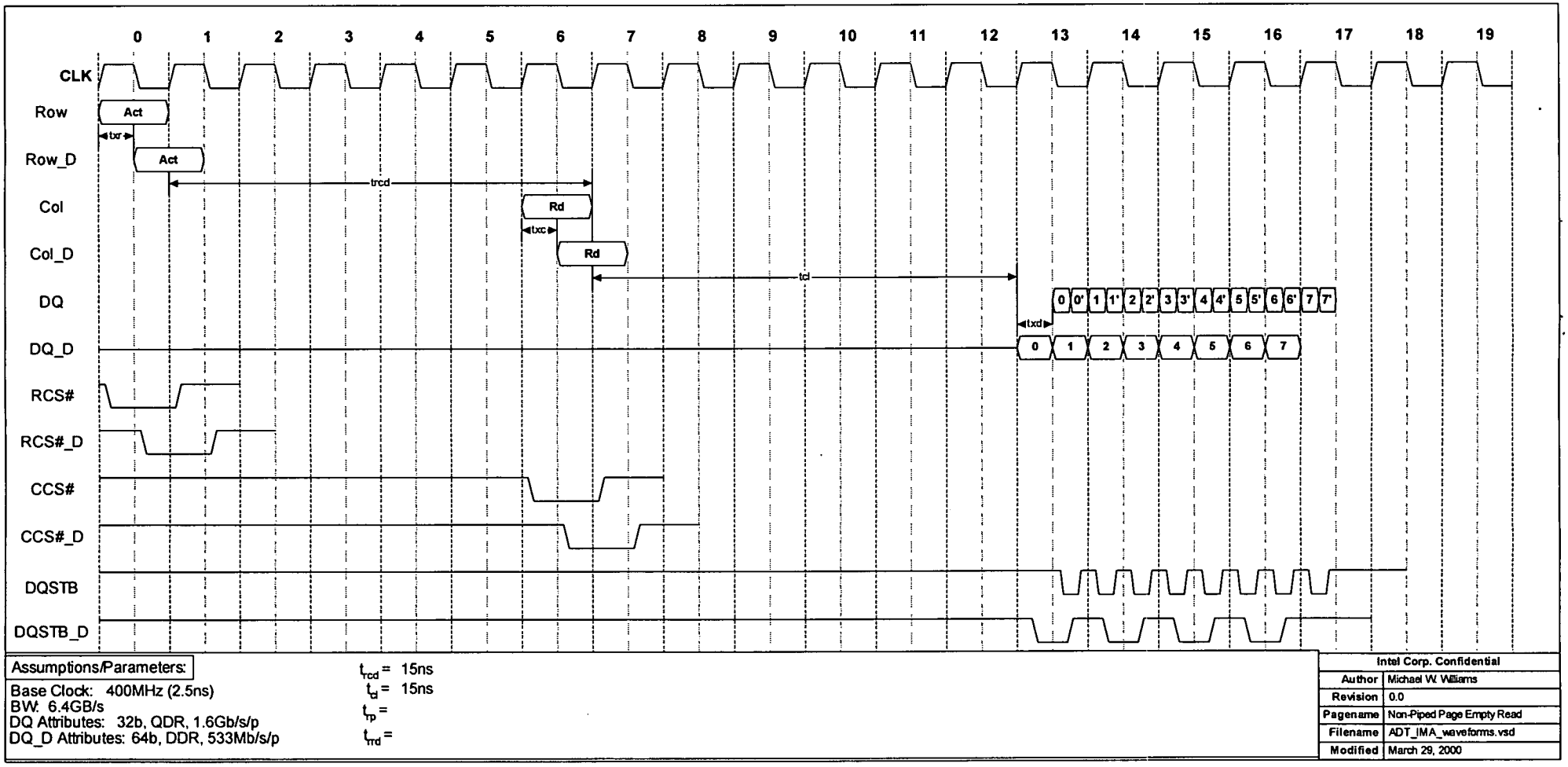
Assumptions/Parameters:

Base Clock: 400MHz (2.5ns)
BW: 6.4GB/s
DQ Attributes: 32b, QDR, 1.6Gb/s/p
DQ_D Attributes: 64b, DDR, 533Mb/s/p

t_{rcd} = 15ns
t_{cl} = 15ns
t_{rp} =
t_{rrd} =

Intel Corp. Confidential

Author	Michael W. Williams
Revision	0.0
Pagename	Page Hit Read Stream
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000



Assumptions/Parameters:

Base Clock: 400MHz (2.5ns)
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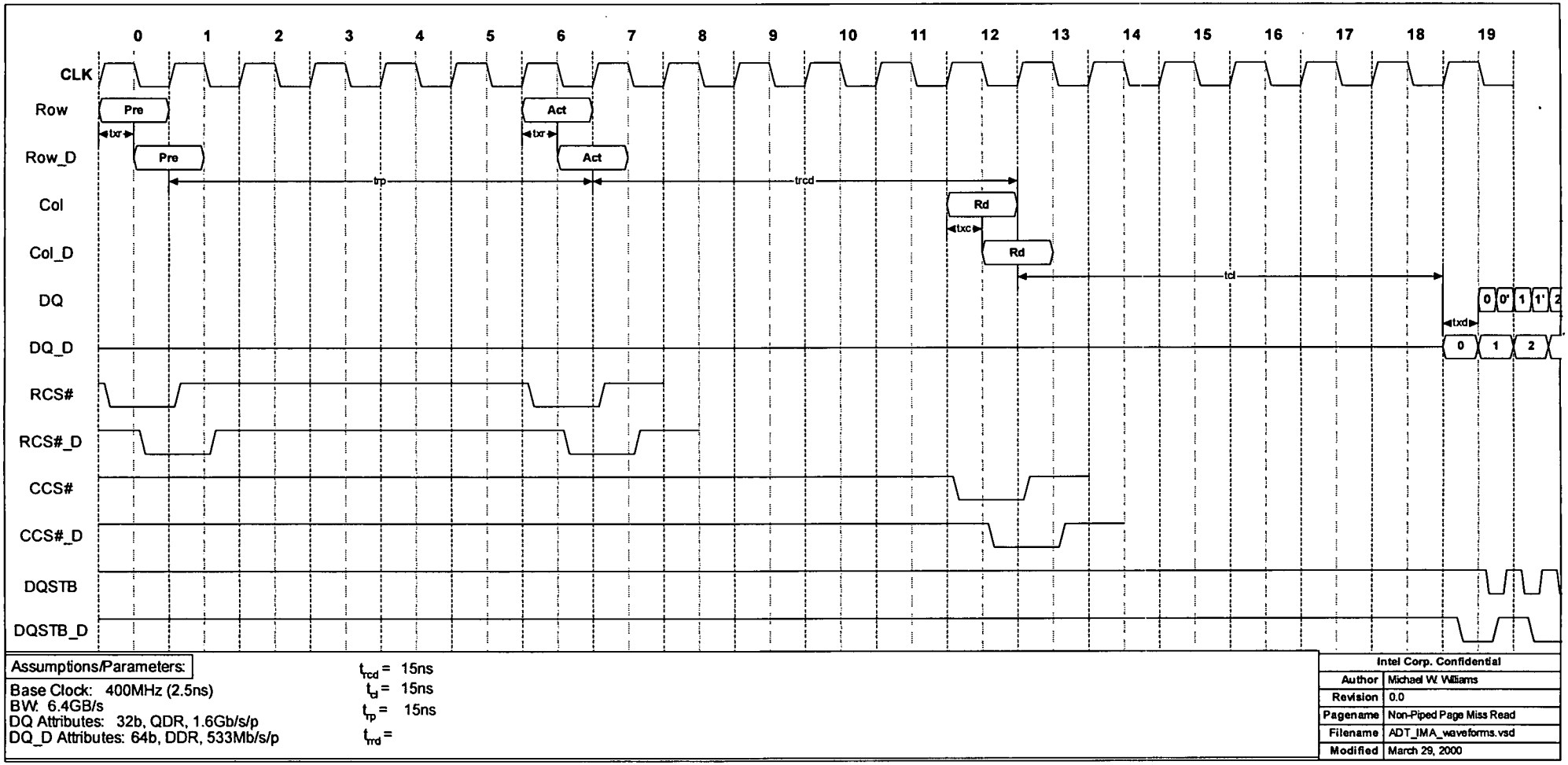
Intel Corp. Confidential	
Author	Michael W. Williams
Revision	0.0
Pagename	Non-Piped Page Empty Read
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000



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t_{rcd} = 15ns
t_{cl} = 15ns
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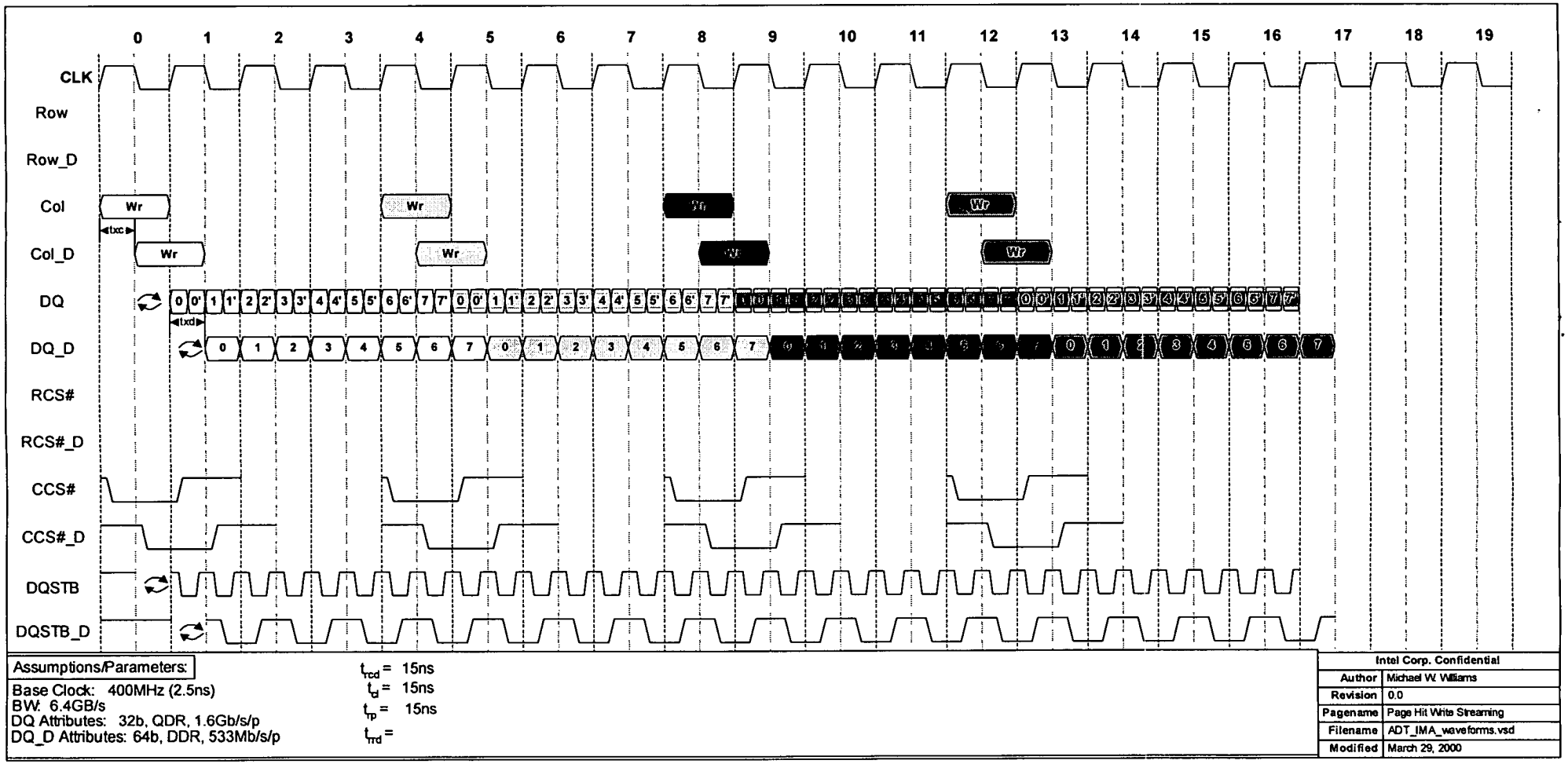
Intel Corp. Confidential	
Author	Michael W. Williams
Revision	0.0
Pagename	Non-Piped Page Miss Read
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000

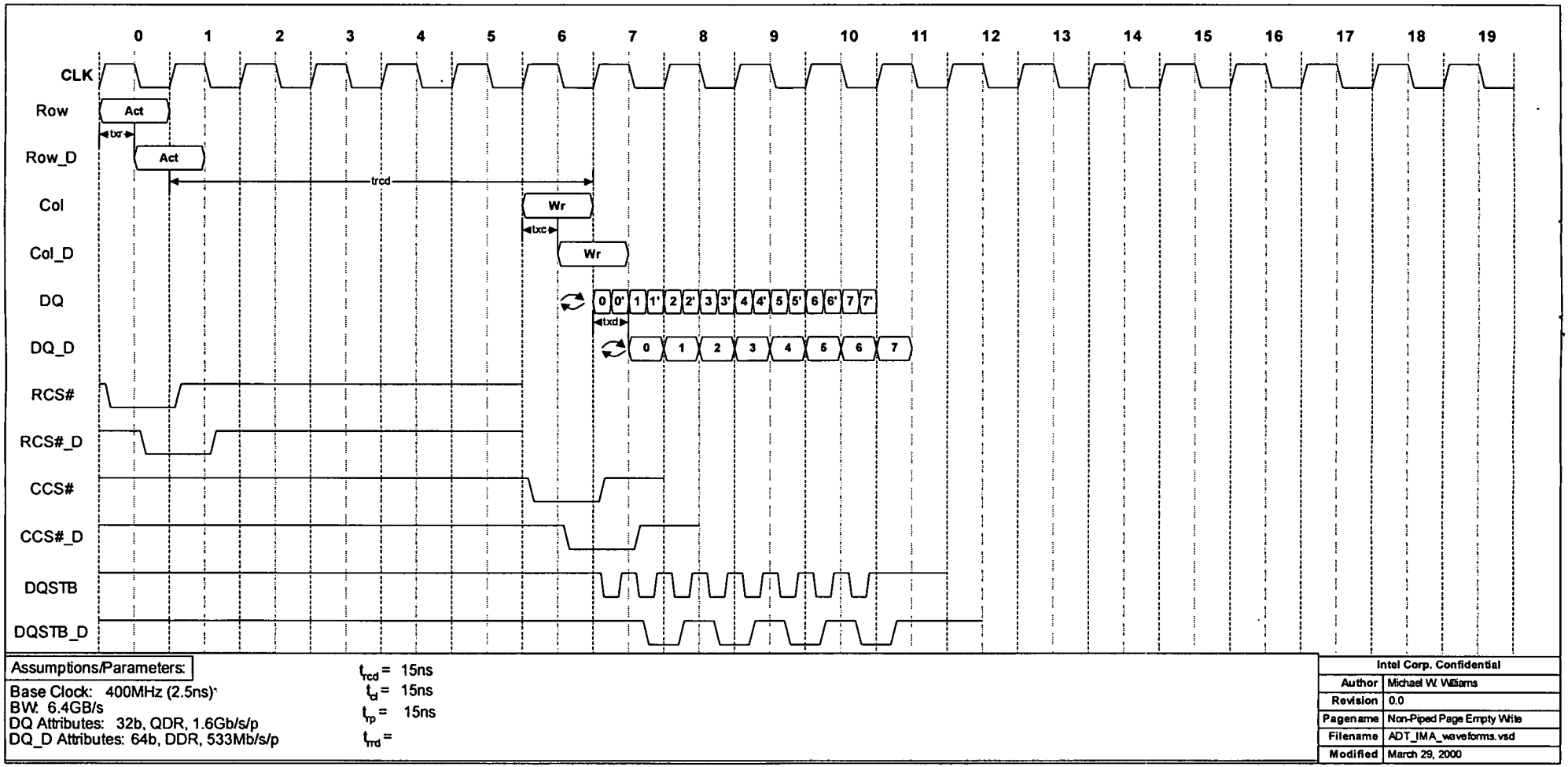


Assumptions/Parameters:

Base Clock: 400MHz (2.5ns)
BW: 6.4GB/s
DQ Attributes: 32b, QDR, 1.6Gb/s/p
DQ_D Attributes: 64b, DDR, 533Mb/s/p

t_{rcd} = 15ns
t_{cl} = 15ns
t_{rp} = 15ns
t_{rrd} =

Intel Corp. Confidential	
Author	Michael W. Williams
Revision	0.0
Pagename	Page Hit Write Streaming
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000

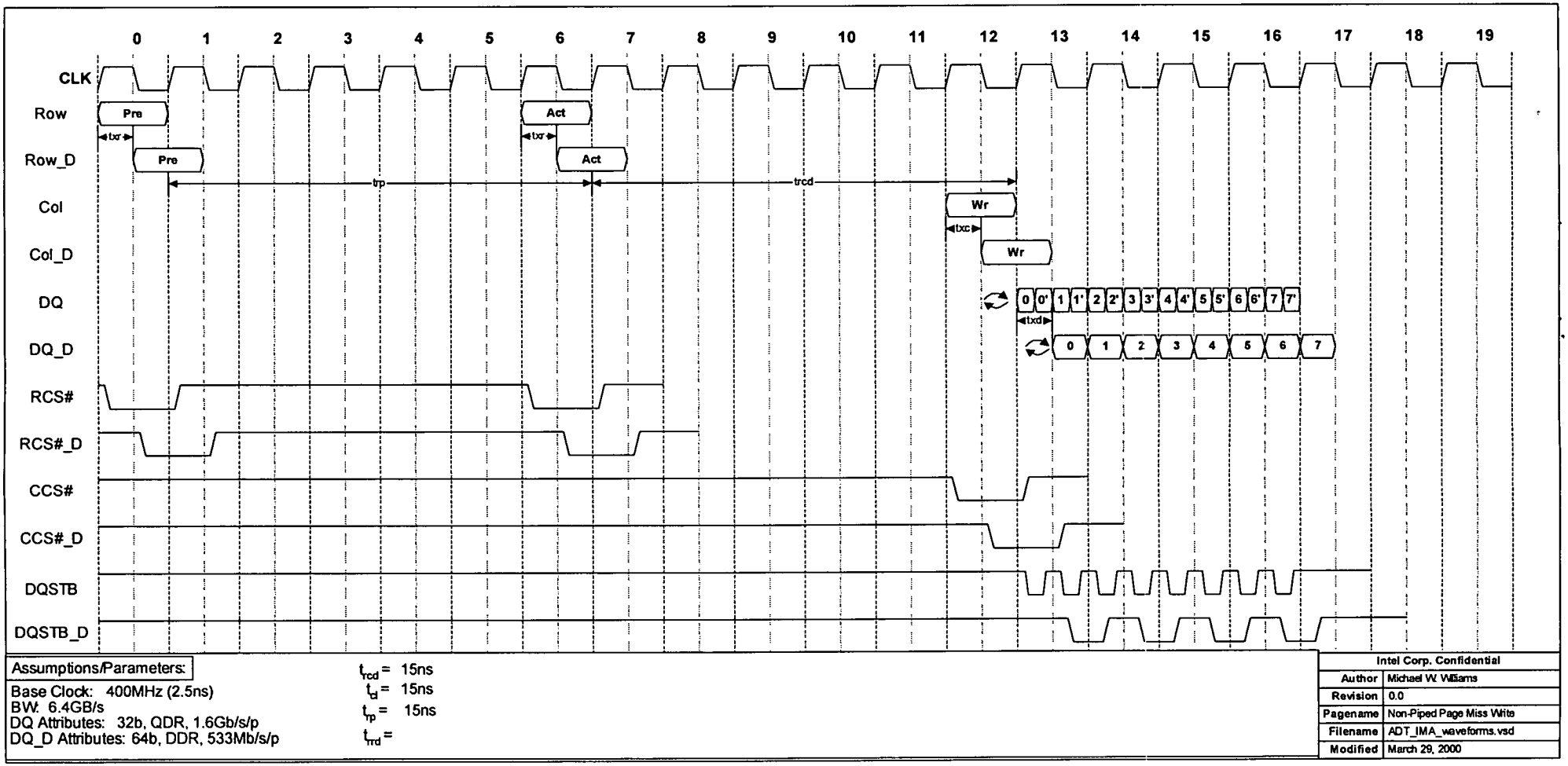


Assumptions/Parameters:

Base Clock: 400MHz (2.5ns)
BW: 6.4GB/s
DQ Attributes: 32b, QDR, 1.6Gb/s/p
DQ_D Attributes: 64b, DDR, 533Mb/s/p

t_{rcd} = 15ns
t_{cl} = 15ns
t_{rp} = 15ns
t_{rrd} =

Intel Corp. Confidential	
Author	Michael W. Williams
Revision	0.0
Pagename	Non-Piped Page Empty Write
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000



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Base Clock: 400MHz (2.5ns)
BW: 6.4GB/s
DQ Attributes: 32b, QDR, 1.6Gb/s/p
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t_{rcd} = 15ns
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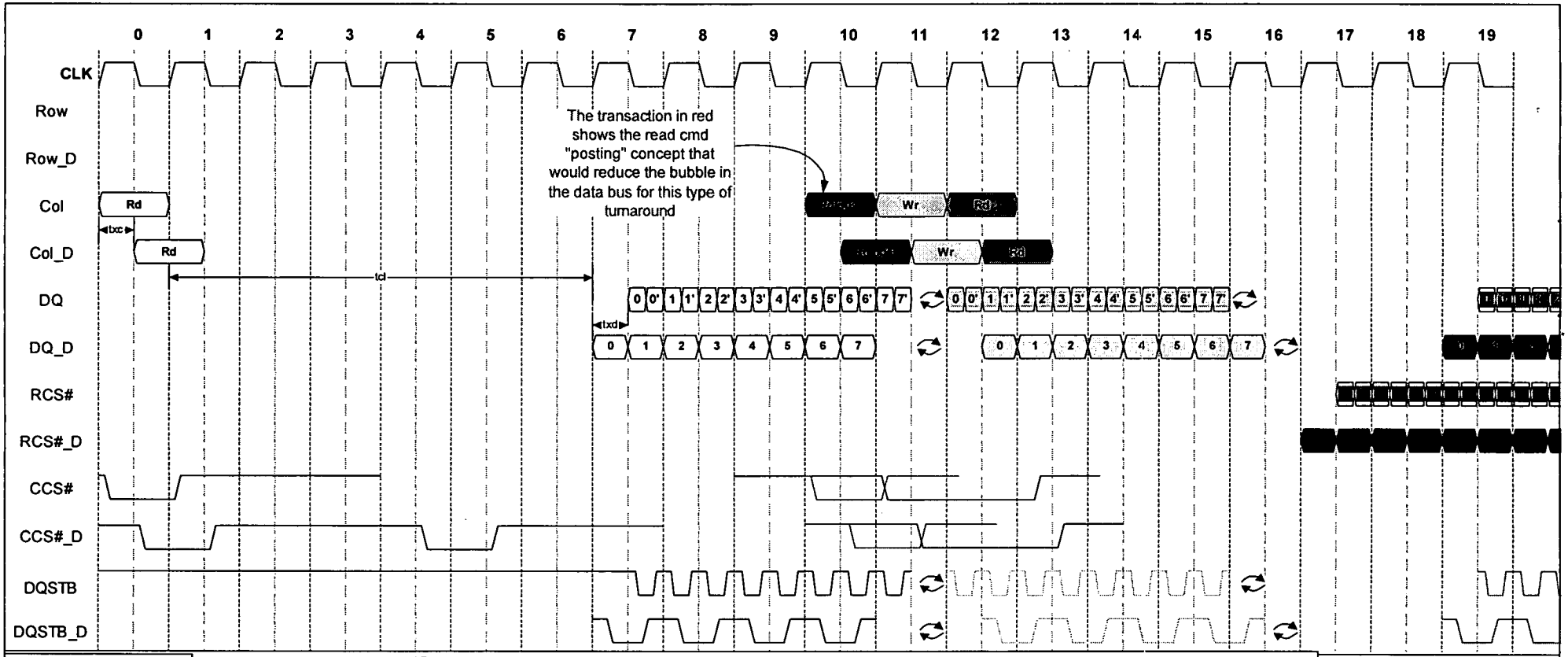
Intel Corp. Confidential	
Author	Michael W. Williams
Revision	0.0
Pagename	Non-Piped Page Miss Write
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000



Assumptions/Parameters:

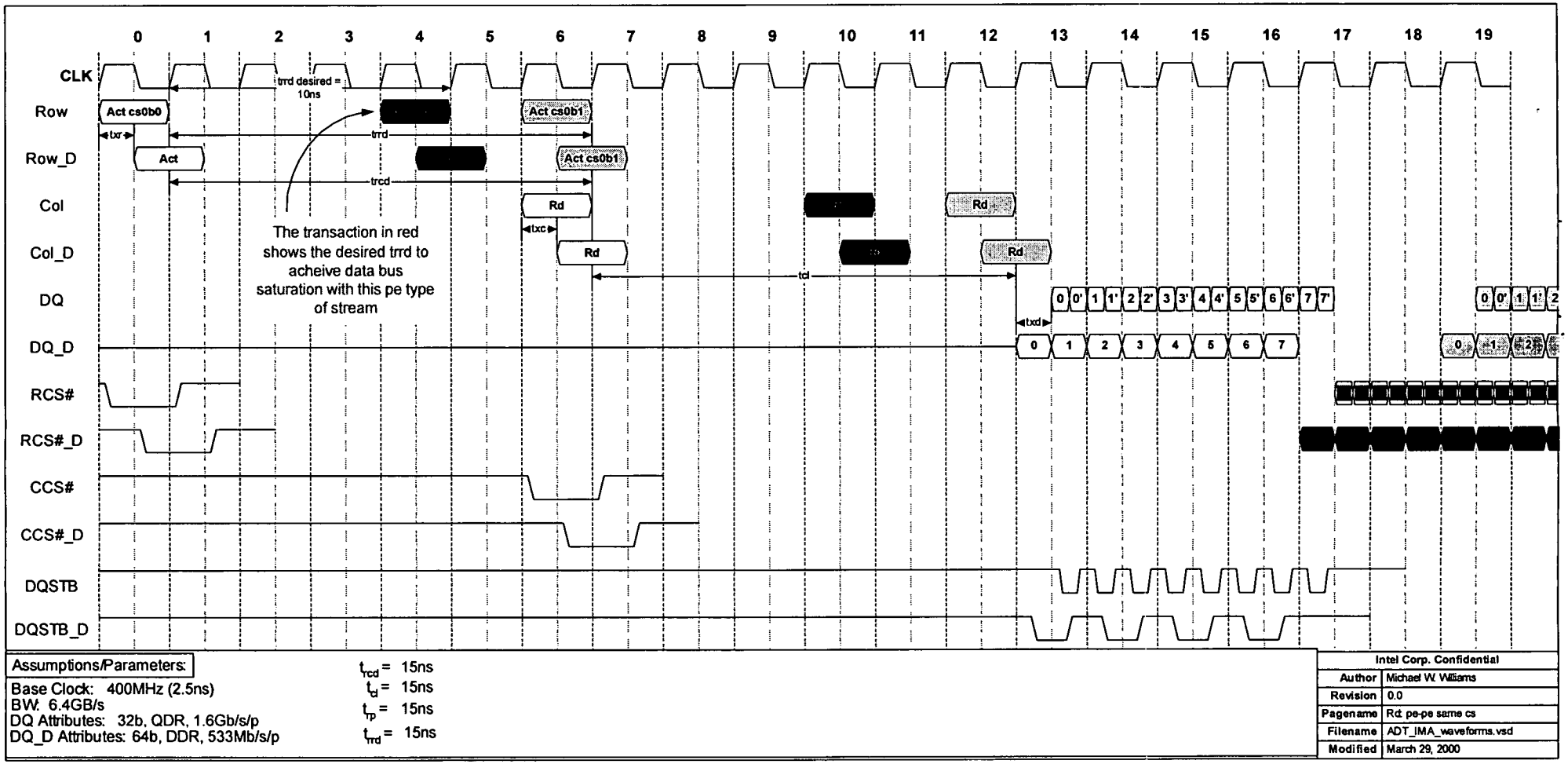
Base Clock: 400MHz (2.5ns)
BW: 6.4GB/s
DQ Attributes: 32b, QDR, 1.6Gb/s/p
DQ_D Attributes: 64b, DDR, 533Mb/s/p

t_{rcd} = 15ns
t_{cl} = 15ns
t_{rp} =
t_{rrd} =

Three Options for bidirect control:

1) count from last read cmd: con- adds ima complexity. pro- not in crit path
2) decode from wr cmd: con- in crit path. pro- simple conceptually
3) discrete control with timing same as or prior to wr cmd: con- adds pin(s). pro- flexible & simple conceptually

Intel Corp. Confidential	
Author	Michael W. Williams
Revision	0.0
Pagename	Rd-Wr-Rd Page Hit Turnarounds
Filename	ADT_IMA_waveforms.vsd
Modified	March 29, 2000


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
CLK
Row
Row_D
Col
Col_D
DQ
DQ_D
RCS#
RCS#_D
CCS#
CCS#_D
DQSTB
DQSTB_D
trrd desired = 10ns
Act cs0b0
Act cs0b1
txr
trrd
Act
trcd
Rd
txc
tcl
txd
The transaction in red shows the desired trrd to acheive data bus saturation with this pe type of stream
Assumptions/Parameters:
Base Clock: 400MHz (2.5ns)
BW: 6.4GB/s
DQ Attributes: 32b, QDR, 1.6Gb/s/p
DQ_D Attributes: 64b, DDR, 533Mb/s/p
t_{rcd} = 15ns
t_{cl} = 15ns
t_{rp} = 15ns
t_{rrd} = 15ns
Intel Corp. Confidential
Author | Michael W. Williams
Revision | 0.0
Pagename | Rd pe-pe same cs
Filename | ADT_IMA_waveforms.vsd
Modified | March 29, 2000